NANO LETTERS

Letter

pubs.acs.org/NanoLett

Direct Growth of Graphene Nanoribbons for Large-Scale Device Fabrication

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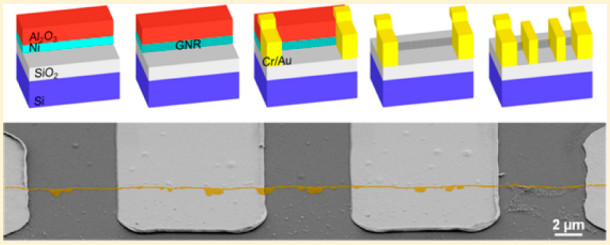
Supporting Information

ABSTRACT: Graphene being a zero band gap material hinders the use of its intrinsic form for many applications requiring a moderate band gap, such as field effect transistors and optoelectronic devices. Here we demonstrate a scalable method based on chemical vapor deposition for the direct growth of well-registered graphene nanoribbons on SiO_2 substrates with precise control over their width, length, and position. The width of the graphene nanoribbons (~20 nm) is defined by the thickness of catalyst film, therefore avoiding the diffraction limit of conventional optical lithographic methods. The carrier mobility (over 1000 $cm^2/V{\cdot}s$) is higher than those previously reported graphene nanoribbons fabricated on SiO_2 substrates, thanks to the present transfer-free and contaminant-free direct growth process. This method overcomes many practical limitations of the previously demonstrated methods for the patterning of graphene nanoribbons and is compatible with large-scale fabrication of graphene nanoelectronics.



KEYWORDS: *Graphene nanoribbons, chemical vapor deposition, transistors, large scale fabrication*

Graphene is an exciting material with great potential for future high-speed and low-power electronics due to its exceptional electronic properties.[1−3] However, the fact that it is a zero band gap material requests the development of fabrication methods to engineer a tunable band gap to develop the applications where such a band gap is required. Different technological approaches have been demonstrated for the opening of such a band gap in graphene, including the use of bilayer graphene device structures,[4] applying strain to graphene,[5] patterning of graphene nanomeshes,[6] or patterning of graphene nanoribbons.[7−16] However, at this point, none of them are practical for graphene device processing because of various technological issues that limit the scales of the processes.

In the case of graphene nanoribbons (GNRs), quasi one-dimensional (1D) graphene strips, both theoretical and experimental results have demonstrated that the band gap of a GNR scales with the inverse of its width and that it is also strongly dependent on the atomic structure of its edges.[10,14,15,17−20] A very narrow (typically a single-digit nanometer width) GNR with clean edges is needed to open a big enough band gap to achieve the high on/off current ratio required for nanoelectronics.[1,3] However, most of the reported approaches for the GNR patterning cannot satisfy the requirements on the precise controls over the width, the edges, and the scalability of the process. For example, the most straightforward method for GNR fabrication consists in the slicing up of a predeposited graphene film, typically by lithographic methods and plasma etching,[8,11,14,15,21,22] but these methods are limited by the difficulty to pattern widths below 10 nm due to the resolution limit of lithography.[14,15] Furthermore, these methods usually produce rough GNR edges that reduce the carrier mobility and deteriorate the device performance significantly.[19,20] The scaling up of these processes requires direct growth or transfer of a single crystalline graphene film on a wafer-size substrate, which is difficult to achieve at this point of the technology. Although the patterning of GNRs at selective facets of silicon carbide (SiC) substrates can potentially produce high quality GNRs,[13] the costly SiC substrate itself is not economically compatible with the large-scale processing in the mainstream semiconductor industry. On the other hand, the liquid phase based approaches, such as the sonochemical processing of carbon nanotubes[9] and graphite,[10] or the metal-surface-assisted coupling of molecular precursors,[12] can also produce high quality GNRs. However, these GNRs still need to be transferred to a proper substrate with a precise alignment and registry control, which is the same unsolved problem that carbon nanotube-based electronics has been facing for many years. Recently, a novel process based on the growth of graphene after the dewetting of Ni nanobars has been reported.[16] However, this process faces the challenges to pattern the Ni nanobar catalysts, the difficulty to control the dewetting, and also the difficulty to find a chemistry to grow the graphene only at one of the facets of the nanobar but not all around it.[23,24] Thus, a method for the patterning of GNRs with

Received: August 10, 2012
Revised: November 4, 2012
Published: November 7, 2012

   dx.doi.org/10.1021/nl302993m | *Nano Lett.* 2012, 12, 6175−6179

precise control over width, edge, alignment, and registry is still needed for large-scale device fabrication.

In a typical chemical vapor deposition (CVD) process of graphene growth, a catalytic material is required to promote the growth.[23−28] Therefore, where no catalytic-surface is found, no graphene should form. Based on this surface-catalytic-selectivity, we have developed a method that enables the growth of GNRs directly on silicon oxide (SiO_2) substrates with accurate control over their width, length, and position. The method consists of the following steps: (1) Sandwiching a thin catalyst layer between the SiO_2 substrate and a top protection layer. (2) Exposing the cross-sectional surface of the catalyst layer by lithography. Here, the width of the exposed surface (nanotemplate) is defined by the catalyst film thickness, hence not by the lithographic resolution. (3) Growth of graphene only at the narrow nanotemplate of the vertically exposed catalyst surface. During this process, the top noncatalytic protection layer not only confines GNR formation, but also prevents the catalytic-layer from dewetting into particles,[25] therefore maintaining the continuity of the catalyst nanotemplate.

Based on this approach, we designed a process for the fabrication of back-gated GNR field effect transistor (FET) test structures. Figure 1 shows the schematics of the major steps of the process for the direct growth of the GNRs (Figure 1a−c) and for the subsequent fabrication of the test structures (Figure 1d−f). In this case, we evaporated a 20 nm thick nickel (Ni) thin film and a 75 nm thick alumina (Al_2O_3) film on a silicon/silicon oxide (n++/∼300 nm) substrate to act as the catalytic and the noncatalytic top protection layer, respectively. Ni and Al_2O_3 were selected because of their high melting points[25] and the stability of their interfaces at the graphene growth temperatures. Photolithography followed by wet chemical etching (H_3PO_4/HNO_3) was used to pattern the Ni/Al_2O_3 multilayer to define the Ni nanotemplates. The CVD growth of graphene was performed at 725 °C and 20 Torr by using ethylene (C_2H_4), hydrogen (H_2), and argon (Ar).[23] Graphene was also simultaneously grown on Ni foil pieces as control samples. The first set of contacts was patterned by photolithography followed by the thermal evaporation of a 10 nm Cr and a 110 nm Au layer and lift-off. Then, the Ni/Al_2O_3 multilayer was removed by wet etching (H_3PO_4/HNO_3). To minimize the GNRs being pulled during this process, gentle stirring was applied, the samples were rinsed in isopropanol after DI water because of its lower surface tension, and they were dried in air. Finally, the second set of contacts was patterned by photolithography, followed by the thermal evaporation of a 10 nm Cr and a 90 nm Au layer, and lift-off.

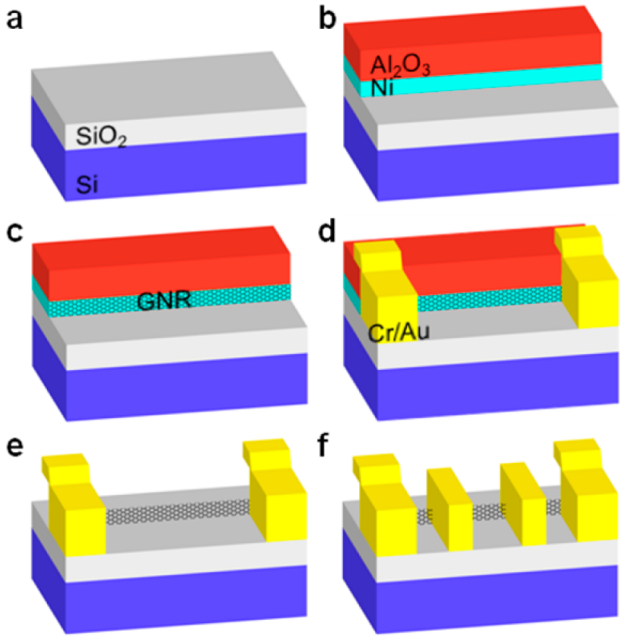


Figure 1. Schematics of the process showing the steps of GNR growth and the test structure fabrication. (a) Silicon−silicon oxide substrate. (b) After patterning Ni/Al_2O_3 multilayer, the Ni cross-section defines the catalytic-surface nanotemplate for the subsequent GNR growth. (c) The surface-catalytic-selectivity of Ni against SiO_2 and Al_2O_3 results in the growth of graphene only at the vertically defined Ni nanotemplate. As-grown GNR stands perpendicular to the SiO_2 substrate. (d) Patterning of the first set of contact electrodes. The registry of the GNR is fixed by these contact electrodes. (e) Removal of the Ni template layer and the Al_2O_3 protection layer by wet etching. (f) Patterning of the second set of contact electrodes.

The technological process was applied to the fabrication of die-scale FET arrays hosting hundreds of devices (Figure 2a shows a block of devices on a die). Figure 2b shows a scanning electron microscopy (SEM) image (Gemini Ultra-55 Analytical from Zeiss) of a long GNR after the contacts had been patterned. Detail of part of the GNR between the central contacts is shown in Figure 2c as measured by atomic force microscopy (AFM; NScriptor AFM from NanoInk Inc.). Since the GNR was grown perpendicular to the substrate, the measured "height" should actually be its "width" by conventional definition, and this "width" is expected to match with the height of the catalyst layer with a <1 nm error.[28] However, on the height profile of the AFM imaging, we determined the "height" of this GNR to be ∼15 nm instead of the ∼20 nm thickness of the deposited Ni catalyst layer. Here, the difference between the GNR width (∼15 nm) and the Ni nanotemplate width (∼20 nm) is most probably due to the bowing of the GNR after the removal of the protection and catalyst layers. Similar widths were measured on other GNRs. The wavy profile of the GNR in these images was due to the use of a low resolution photomask (±0.5 μm feature tolerance) in the Ni and Al_2O_3 multilayer patterning. The profile of the GNR is expected to be straighter after the use of a higher resolution photomask or any other patterning technique resulting in lower patterning tolerances, such as e-beam lithography. The images also show that graphene plateaus grew randomly toward the inside of the Ni and Al_2O_3 multilayer. We believe that these plateaus form at the boundaries between Ni grains at the Ni−Al_2O_3 interface because of the higher diffusion of the carbon atoms[24] and that they can be avoided after the improvement of the Ni and Al_2O_3 deposition and patterning conditions.

Raman spectroscopy (ARAMIS confocal Raman microscope from Horiba, 532 nm laser, spot size: ∼1 μm, power: ∼2.7 mW) was used to evaluate the structural quality of the as-grown GNRs (Figure 3). The observation of the characteristic peaks of graphene only in the local spots (#1 and #2) where the edges of the Ni and Al_2O_3 multilayer patterns located provides the evidence for the formation of the GNRs only on the defined Ni nanotemplates (Figure 3a−c).[29,30] Away from the Ni nanotemplates, the only observed peaks are from the silicon substrate (Figure 3d). The Raman spectra of the GNRs include the D-band (∼1350 cm^{-1}), the G-band (∼1480 cm^{-1}), the D′-band (∼1620 cm^{-1}), and the 2D band (∼2690 cm^{-1}) (Figure 3d). Based on the analyses of the 2D bands, we estimated that

dx.doi.org/10.1021/nl302993m | Nano Lett. 2012, 12, 6175−6179

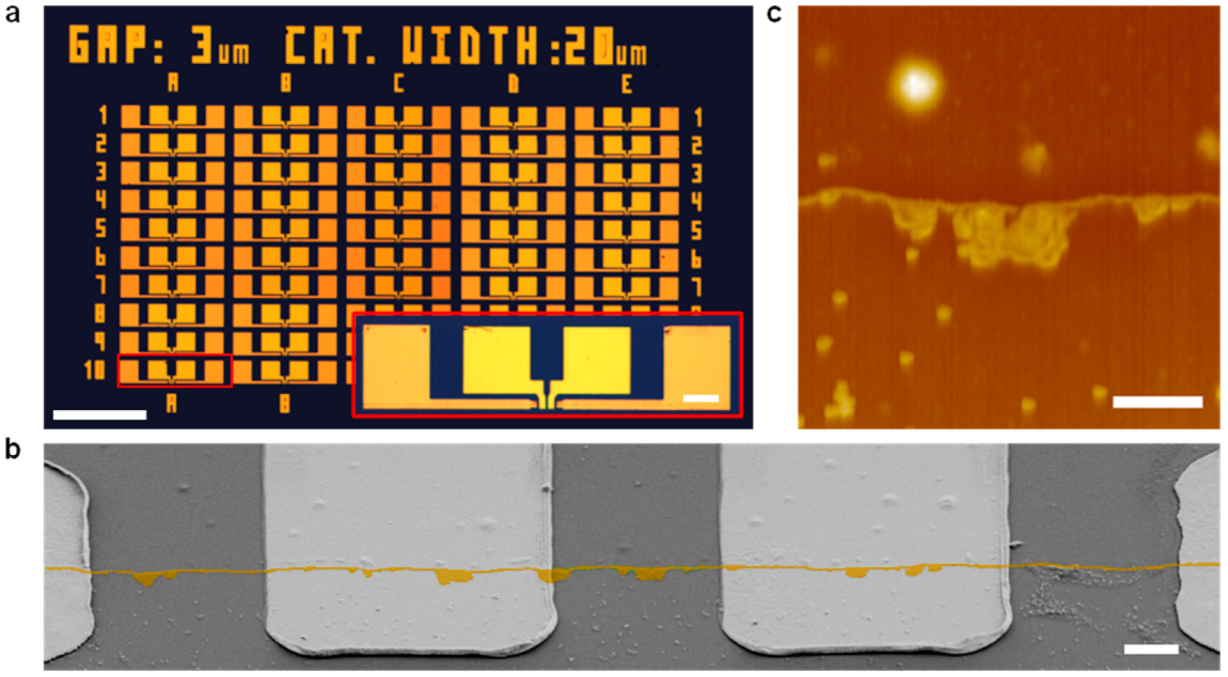


Figure 2. GNR-FET array test structure. (a) Optical images of an GNR-FET array consisting of 50 devices. Each GNR in the FET device is contacted by four metal electrodes in a four-point configuration (inset). Scale bars are 500 and 50 μm (inset), respectively. (b) SEM image of a GNR after the two sets of metal electrodes had been patterned. The GNR has been artificially colored for a clearer presentation. In this case, the nominal gap between the central electrodes is 7 μm. A small amount of residues can be identified in the area below the GNR, where the Ni/Al_2O_3 pattern had been removed after graphene growth. The scale bar is 2 μm. (c) A topographic AFM image of the GNR section between the central electrodes in panel b. The image shows the GNR as well as the graphene plateaus that formed at the Ni/Al_2O_3 interface. The scale bar is 1 μm.

the GNRs consisted of 3−5 graphene layers in agreement with the control samples of the graphene films grown on Ni foils.[29,31] The intensity of the G and 2D bands was strongly dependent on whether the sampling occurred on a GNR or on a plateau, due to the smaller amount of irradiated *sp*2 bonds in the former case.[11,21,22] However, no dependence on the D band intensity was observed since the irradiated edge length was similar because of the large diameter of the laser spot. Besides, we observed a shift of the G and 2D bands from the graphene plateaus with respect to those from the GNRs. We relate this shift to the strain that appears on the graphene plateaus when they become suspended after the removal of the Ni layer.[32] Therefore, this shift confirms that the plateaus form only at the Ni/Al_2O_3 interface. The D/G band ratios of our GNRs suggest that their edges could be less defective than previously reported oxygen plasma patterned GNRs of similar width,[21,22] though a quantitative comparison is not possible because of the different experimental setups.[22,33] Based on the barrier-guided growth of graphene process, a similar process to the one described here, better edge quality than that of GNRs that have been patterned by dry etching of graphene and, possibly, edges showing a preferential growth structure should be expected.[28]

The electrical testing of the fabricated GNR-FET devices was also performed. First, a fast 2-probe screening of the drain-source current (I_{DS}) versus the gate voltage (V_{GS}) test (V_{DS} = 0.3 V, V_{GS}: −20, 20 V) served to evaluate the fabrication yield, that is, the yield on the continuity of the GNR over the channel length, to be ∼60% and ∼30% for devices with 3 and 7 μm channel lengths, respectively. Thus, if devices based on GNR lengths smaller than 3 μm were fabricated, a device fabrication yield higher than 60% shall be envisioned. After the fabrication yield screen test, the chips were pumped down to high vacuum (4.5×10^{-5} Torr) and thermally annealed (100 °C, 30 min). Then selected devices were tested in a 4-probe configuration (4156C semiconductor parameter analyzer from Agilent). After the patterning of a 20 nm GNR an energy gap ∼50 meV is expected ($E_g \approx 1/\text{width}$).[10,14,16,17] The energy gap being higher than the thermal voltage enabled its observation at room temperature. Figure 4 depicts the electrical characteristics of a representative GNR-FET device at room temperature. The topographic AFM image of the device is shown as the inset. The characteristics of our GNR-FET are comparable to those of previously reported GNR-FET devices with similar GNR widths.[11,15] Under the above-described conditions, the on/off current ratio was typically recorded to be around 2. The noise on the *IV* characteristics is attributed to impurities close to the GNR[34] resulting from a too-gentle stirring of the sample during the wet processing to inhibit the pulling down of the GNRs. Based on its morphology and on its IV characteristics, the mobility of this GNR was estimated to be higher than 1000 $cm^2/V{\cdot}s$ (see Supporting Information). This mobility value is among the highest values for analogous previously reported GNR-FET devices (in terms of the GNR width and the GNR-FET processing)[10] and on the same order to that reported for GNRs directly grown on SiC substrates.[13] On one hand, this mobility should be attributed to a high quality of the GNR edges, which is achieved by the direct surface-selective-growth of the graphene, and to the process not requiring the transfer of graphene, which generates less defects or ripples.[35,36] On the other hand, the mobility should also benefit from the minimized interfacial scattering due to the fact that there is no contaminant trapped at the GNR-SiO_2 interface as the GNR stands perpendicular to the substrate.[37]

Our method based on the surface-selective growth of graphene for GNR growth has many advantages over the previous GNR fabrication methods. First, it enables the tunable

dx.doi.org/10.1021/nl302993m | *Nano Lett.* 2012, 12, 6175−6179

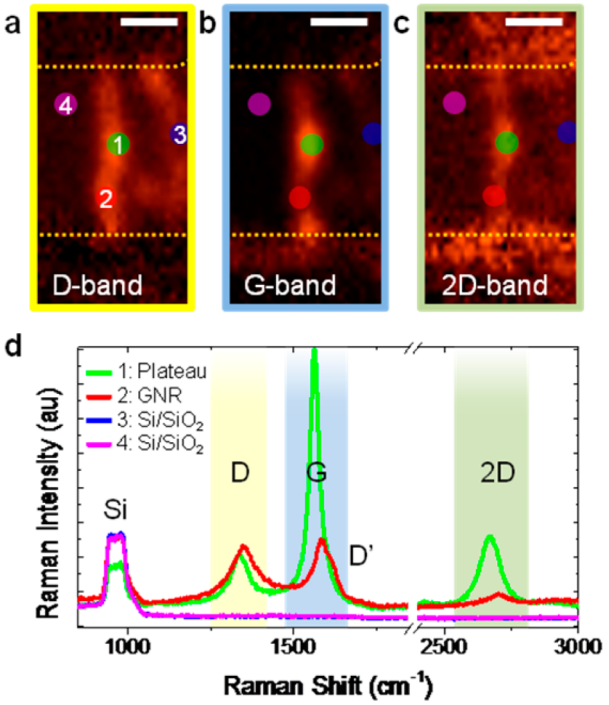


Figure 3. Raman characterization of the GNR test structures. (a–c) Raman mapping of the D, G, and 2D-bands of the GNR in Figure 2c. The mapping images show a broadened feature size of the GNR compared to the previous SEM and AFM images (Figure 2b and c). This is due to the spatial oversampling of the Raman laser which has a spot size (~1 μm) much larger than the width of the GNR and the size of the graphene plateaus. The maps have been rotated 90° with respect to Figure 2c. The dashed lines indicate the boundaries of the metal electrodes. Scale bars are 2 μm. (d) Confocal Raman spectra acquired at the local spots shown in a–c. The Raman signals are collected within the diameter of the confocal laser spot (~1 μm).

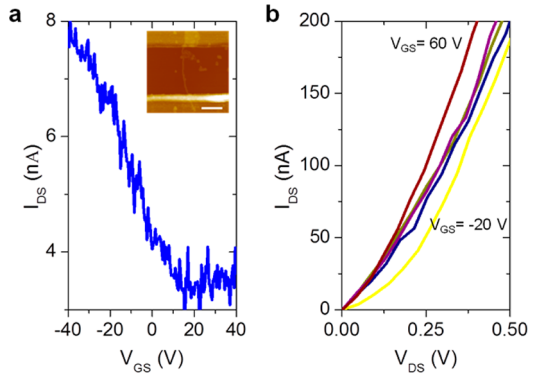


Figure 4. Electrical testing of the GNR-FET test structures. (a) I–V_{GS} (V_{GNR} = 20 mV) and (b) I_{DS}–V_{DS} (V_{GS} keeps at −20 V, 20 V, 40 V, and 60 V, respectively.) Current-bias characteristics obtained from the GNR-FET device as shown in the inset of a, under a 4-point probing configuration. GNR width is determined as 20 nm by the AFM topographic imaging. GNR channel length: 2.4 μm between inner contacts (channel length), and 29 μm between outer contacts of the 4-point test structure (see inset in Figure 2a), respectively. The scale bar in the AFM image is 1 μm.

width growth of GNRs since the nanotemplates are controlled after the thickness of the catalytic material layer. Therefore, if the layer was scaled down to an only few angstroms thickness, GNRs with band gaps larger than 0.5 eV or even 1 eV are expected, thus, enabling room temperature GNR-FET based applications. Furthermore, we have shown that the morphology of these nanotemplates defines the length and the position of the GNRs. Here we have validated the process by using Ni and Al_2O_3 as the catalytic and noncatalytic materials, respectively, but the method is compatible with any other catalytic/noncatalytic material combination as long as their interfaces are stable during the processing. Regarding the quality of the GNRs, on the one side, the formation of ripples and the defects that originate after graphene transfer are avoided by our method. On the other side, we believe that achieving atomically precise interfaces between the catalytic and noncatalytic surfaces will minimize the formation of graphene plateaus, thus, leading to the growth of GNRs with atomically precise edges. Last, since the fabrication steps for the patterning of the GNRs are compatible with standard fabrication techniques and since we have demonstrated that the resulting GNRs are compatible with the postgraphene-growth processes for circuit integration, this method can be scaled to substrates of arbitrary sizes. Further studies will be needed in the future to address the optimization of the anchoring of the GNR to the substrate during the wet etching of the catalytic and the noncatalytic layers, to develop strategies to lie the GNR down onto the substrate, to determine the scaling limits of the process, and to elucidate the structural, mechanical, thermal,[38] and electrical properties and limitations of the GNRs.

In conclusion, we report on a method that overcomes the practical limitations for the patterning of GNRs with precise control over their width, and position, and for the scalability of the process. Therefore, this method may pave the way to the successful integration of GNRs into nanoelectronics.

■ ASSOCIATED CONTENT

Supporting Information

Carrier mobility calculation method. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

The authors thank Drs. Tevye Kuykendall, Emory Chan, Richa Sharma and Nelson Coates for assistance on the growth and the characterization of the GNR and the test structures, and Dr. Stefano Cabrini and his group for discussion and support on the technological processing. This work was supported by the Office of Science, Office of Basic Energy Sciences of the U.S. Department of Energy under contract no. DE-AC02-05CH11231.

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